

# DATA SHEET

## **TDA1541** Dual 16-bit DAC

Product specification  
File under Integrated Circuits, IC01

November 1985

## Dual 16-bit DAC

## TDA1541

## GENERAL DESCRIPTION

The TDA1541 is a monolithic integrated dual 16-bit digital-to-analogue converter (DAC) designed for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders.

## Features

- Selectable two-channel input format: offset binary or two's complement
- Internal timing and control circuit
- TTL compatible digital inputs
- High maximum input bit-rate and fast settling time.

## QUICK REFERENCE DATA

Supply voltages				
pin 28	$V_{DD}$	typ.	5	V
pin 26	$V_{DD1}$	typ.	-5	V
pin 15	$V_{DD2}$	typ.	-15	V
Supply currents				
pin 28	$I_{DD}$	typ.	45	mA
pin 26	$I_{DD1}$	typ.	45	mA
pin 15	$I_{DD2}$	typ.	25	mA
Signal-to-noise ratio (full scale sine-wave)				
at analogue outputs (AOL; AOR)	S/N	typ.	95	dB
Non-linearity at $T_{amb} = -20$ to $+70$ °C				
		typ.	$\frac{1}{2}$	LSB
Current settling time to $\pm 1$ LSB				
	$t_{cs}$	typ.	1	$\mu$ s
Maximum input bit rate at data input (pin 3)				
	$BR_{max}$	min.	6	Mbits/s
Maximum clock frequency at clock input (pin 2)				
	$f_{BCKmax}$	min.	6	MHz
at clock input (pin 4)				
	$f_{SCKmax}$	min.	12	MHz
Full scale temperature coefficient at analogue outputs (AOL; AOR)				
	$TC_{FS}$	typ.	$\pm 200 \times 10^{-6}$	$K^{-1}$
Operating ambient temperature range				
	$T_{amb}$		-20 to +70	°C
Total power dissipation				
	$P_{tot}$	typ.	850	mW

## PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT-117); SOT117-1; 1996 August 14.



# Dual 16-bit DAC

# TDA1541

### PINNING

1	LE/WS*	latch enable input word select input
2	BCK*	bit clock input
3	DATA L/DATA*	data left channel input data input (selected format)
4	DATA R/SYS*	data right channel input system clock input
5	GND (A)	analogue ground
6	AOR	right channel output
7	DECOU	decoupling
8	DECOU	
9	DECOU	
10	DECOU	
11	DECOU	
12	DECOU	
13	DECOU	
14	GND (D)	digital ground
15	V <sub>DD2</sub>	-15 V supply voltage
16	n.c.	not connected
17	n.c.	
18	DECOU	decoupling
19	DECOU	
20	DECOU	
21	DECOU	
22	DECOU	
23	DECOU	
24	DECOU	
25	AOL	left channel output
26	V <sub>DD1</sub>	-5 V supply voltage
27	OB/TWC*	mode selection input
28	V <sub>DD</sub>	+5 V supply voltage

\* See Table 1 data selection input.

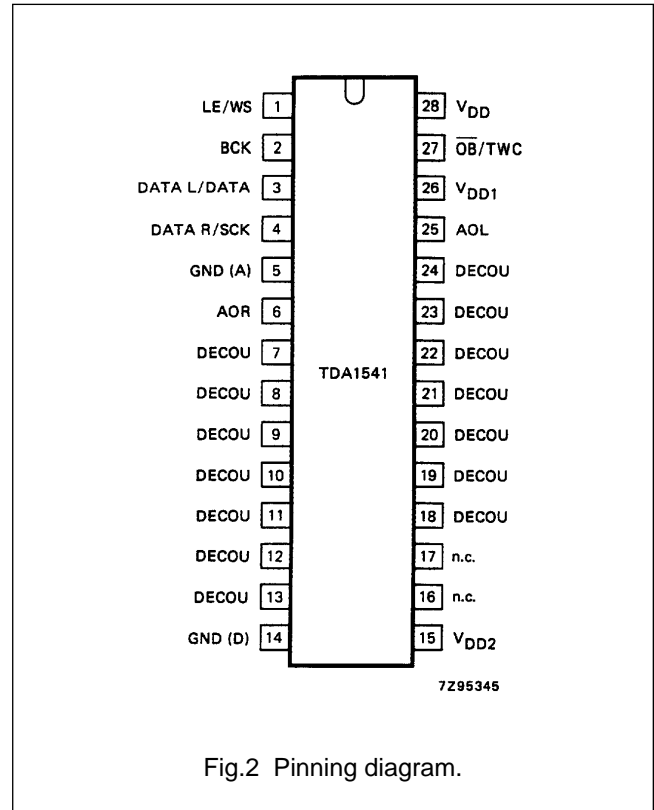


Fig.2 Pinning diagram.

## Dual 16-bit DAC

## TDA1541

**FUNCTIONAL DESCRIPTION**

The TDA1541 accepts input sample formats in time multiplexed mode or simultaneous mode with any bit length. The most significant bit (MSB) must always be first. This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit-rate and fast settling time facilitates application in  $4 \times$  oversampling systems (44,1 kHz to 176,4 kHz) with the associated simple analogue filtering function (low order, linear phase filter).

**Input data selection** (see also Table 1)

With input  $\overline{\text{OB}}/\text{TWC}$  connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. A separate system clock input (SCK) is provided for accurate, jitter-free timing of the analogue outputs AOL and AOR.

With  $\overline{\text{OB}}/\text{TWC}$  connected to  $V_{\text{DD}}$  the mode is the same but data format must be in two's complement.

When input  $\overline{\text{OB}}/\text{TWC}$  is connected to ( $V_{\text{DD}1}$ ) the two channels of data (L/R) are input simultaneously via (DATA L) and (DATA R), accompanied with BCK and a latch-enable input (LE). With this mode selected the data must be in offset binary.

The format of data input signals is shown in figures 3, 4 and 5.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current-divider, based on emitter scaling. All digital inputs are TTL compatible.

**Input data selection**

$\overline{\text{OB}}/\text{TWC}$	MODE	PIN 1	PIN 2	PIN 3	PIN 4
-5 V	simultaneous	LE	BCK	DATA L	DATA R
0 V	time MUX OB	WS	BCK	DATA OB	SCK
+5 V	time MUX TWC	WS	BCK	DATA TWC	SCK

Where:

LE	= latch enable
WS	= word select
BCK	= bit clock
DATA L	= data left
DATA R	= data right
DATA OB	= data offset binary
DATA TWC	= data two's complement
MUX OB	= multiplexed offset binary
MUX TWC	= multiplexed two's complement

## Dual 16-bit DAC

TDA1541

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges

pin 28	$V_{DD}$	0 to +7	V
pin 26	$V_{DD1}$	0 to -7	V
pin 15	$V_{DD2}$	0 to -17	V
Crystal temperature range	$T_{XTAL}$	-55 to +150	°C
Storage temperature range	$T_{stg}$	-55 to +150	°C
Operating ambient temperature range	$T_{amb}$	-20 to +70	°C
Electrostatic handling <sup>(1)</sup>	$V_{es}$	-1000 to +1000	V

**Note**1. Discharging a 250 pF capacitor through a 1 k $\Omega$  series resistor.**THERMAL RESISTANCE**

From junction to ambient	$R_{th\ j-a}$	=	35	K/W
--------------------------	---------------	---	----	-----

## Dual 16-bit DAC

## TDA1541

**CHARACTERISTICS**

$V_{DD} = +5\text{ V}$ ;  $V_{DD1} = -5\text{ V}$ ;  $V_{DD2} = -12\text{ V}$ ;  $T_{amb} = +25\text{ °C}$ ; measured in Fig. 1; unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>					
Supply voltage ranges					
pin 28	$V_{DD}$	4,0	5,0	6,0	V
pin 26	$-V_{DD1}$	4,5	5,0	6,0	V
pin 15	$-V_{DD2}$	14	15	16	V
Supply currents					
pin 28	$I_{DD}$	–	45	tbf	mA
pin 26	$-I_{DD1}$	–	45	tbf	mA
pin 15	$-I_{DD2}$	–	25	tbf	mA
Resolution	Res	–	16	–	bits
<b>Inputs</b>					
Input current (pin 3 and pin 4)					
digital inputs LOW (< 0,8 V)	$I_{IL}$	–	–	tbf	mA
digital inputs HIGH (> 2,0 V)	$I_{IH}$	–	–	tbf	$\mu\text{A}$
Input frequency					
at clock input (pin 4)	$f_{SCK}$	–	–	12	MHz
at clock input (pin 2)	$f_{BCK}$	–	–	6	MHz
at data inputs (pin 3 and pin 4)	$f_{DAT}$	–	–	6	MHz
at word select input (pin 1)	$f_{WS}$	–	–	200	kHz
Input capacitance of digital inputs	$C_i$	–	12	–	pF
<b>Oscillator</b>					
Oscillator frequency					
with internal capacitor	$f_{osc}$	150	200	250	kHz
<b>Analogue outputs (AOL; AOR)</b>					
Output voltage compliance	$V_{OC}$	tbf	–	tbf	mV
Full scale current	$I_{FS}$	3,4	4,0	4,6	mA
Zero scale current	$\pm I_{ZS}$	–	tbf	–	nA
Full scale temperature coefficient	$TC_{FS}$	–	$\pm 200 \times 10^{-6}$	–	$K^{-1}$
Linearity error integral					
at $T_{amb} = 25\text{ °C}$	$E_1$	–	0,5	–	LSB
at $T_{amb} = -20\text{ to }+70\text{ °C}$	$E_1$	–	tbf	–	LSB
Linearity error differential					
at $T_{amb} = 25\text{ °C}$	$E_{d1}$	–	0,5	1	LSB
at $T_{amb} = -20\text{ to }+70\text{ °C}$	$E_{d1}$	–	tbf	–	LSB

## Dual 16-bit DAC

## TDA1541

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Signal -to-noise ratio + THD*	S/N	90	95	–	dB
Settling time to $\pm 1$ LSB	$t_{cs}$	–	1	–	$\mu s$
Channel separation	$\alpha$	80	tbf	–	dB
Unbalance between outputs	$\Delta I_{FS}$	–	0,1	0,2	dB
Time delay between outputs	$t_d$	–	–	1	$\mu s$
Power supply ripple rejection**					
$V_{DD} = +5 V$	RR	–	tbf	–	dB
$V_{DD1} = -5 V$	RR	–	tbf	–	dB
$V_{DD2} = -15 V$	RR	–	tbf	–	dB
Signal-to-noise ratio at bipolar zero	S/N	–	–100	–	dB
<b>Timing</b> (see Figs 3, 4 and 5)					
Rise time	$t_r$	–	–	35	ns
Fall time	$t_f$	–	–	35	ns
Bit clock cycle time	$t_{CY}$	160	–	–	ns
Bit clock HIGH time	$t_{HB}$	48	–	–	ns
Bit clock LOW time	$t_{LB}$	48	–	–	ns
Bit clock fall time to latch rise time	$t_{FBRL}$	0	–	–	ns
Bit clock rise time to latch fall time	$t_{RBFL}$	0	–	–	ns
Data set-up time to bit clock	$t_{SDB}$	32	–	–	ns
Data hold time to bit clock	$t_{HDB}$	0	–	–	ns
Data set-up time to system clock	$t_{SDS}$	32	–	–	ns
Word select hold time to system clock	$t_{HWS}$	0	–	–	ns
Word select set-up time to system clock	$t_{SWS}$	32	–	–	ns
Bit clock fall time to system clock rise time	$t_{FBRS}$	32	–	–	ns
System clock rise time to bit clock fall time	$t_{RSFB}$	32	–	–	ns
System clock fall time to bit clock rise time	$t_{FSRB}$	50	–	–	ns
Bit clock rise time to system clock fall time	$t_{RBFS}$	0	–	–	ns
Latch enable LOW time	$t_{LLE}$	20	–	–	ns
Latch enable HIGH time	$t_{HLE}$	32	–	–	ns

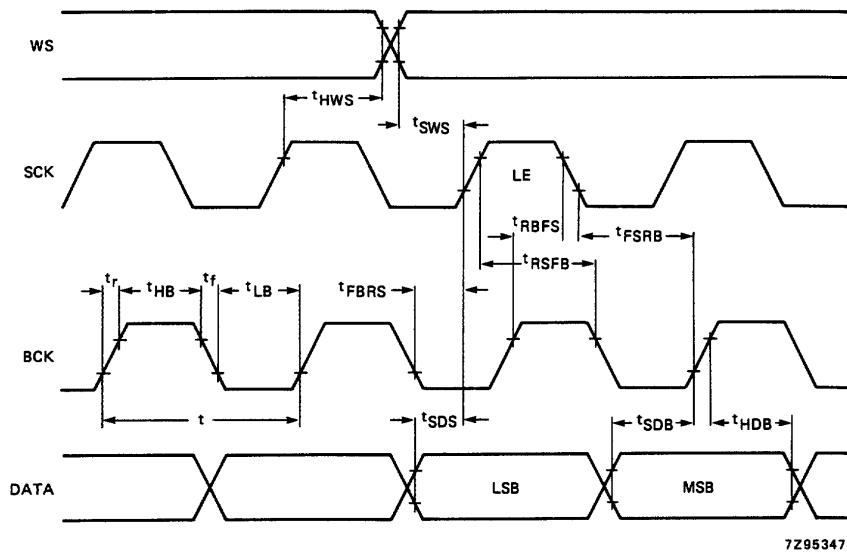
\* Signal-to-noise ratio + THD with 1 kHz full scale sinewave generated at a sampling rate of 176,4 kHz.

\*\*  $V_{ripple} = 1\%$  of supply voltage and  $f_{ripple} = 100$  Hz.



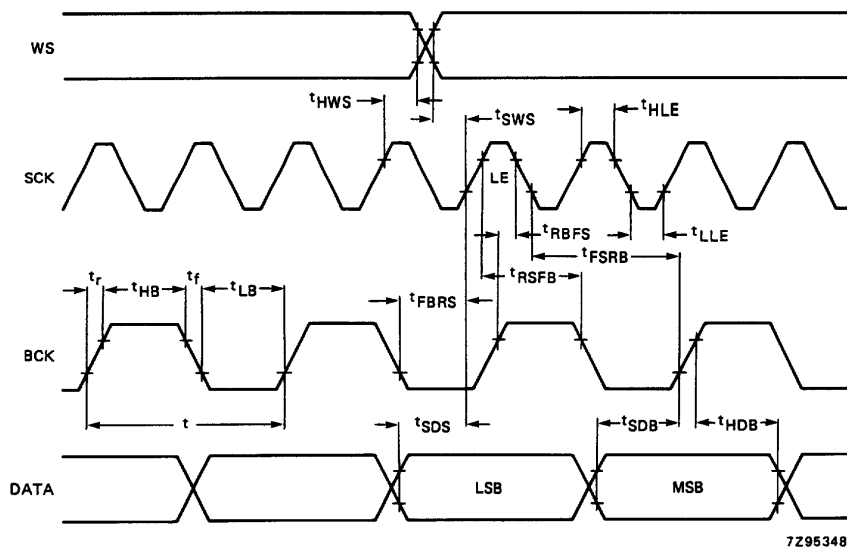
Dual 16-bit DAC

TDA1541



7295347

Fig.3 Format of input signals; time multiplexed at  $f_{SCK} = f_{BCK}$  (I<sup>2</sup>S format).

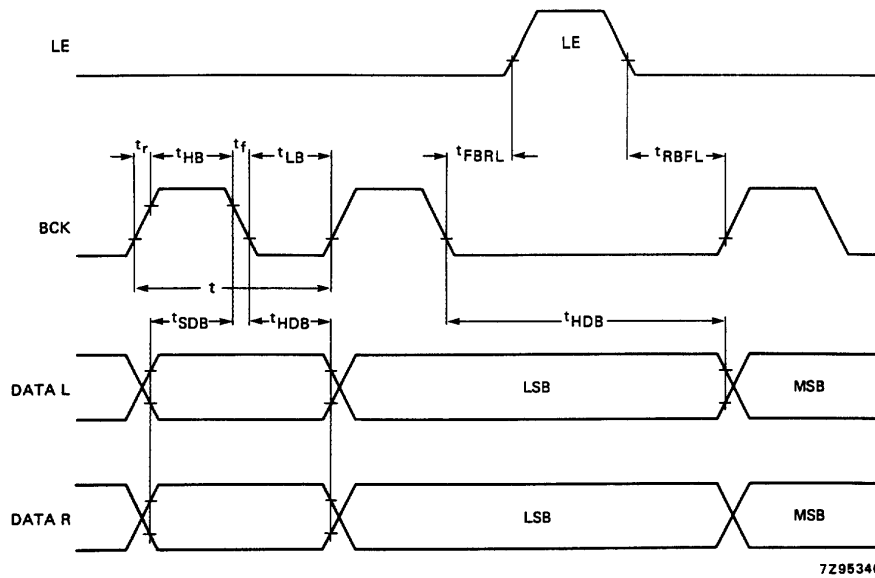


7295348

Fig.4 Format of input signals; **time multiplexed** at  $f_{SCK} = 2 \times f_{BCK}$ .

Dual 16-bit DAC

TDA1541



7295346

Fig.5 Format of input signals; **simultaneous data.**

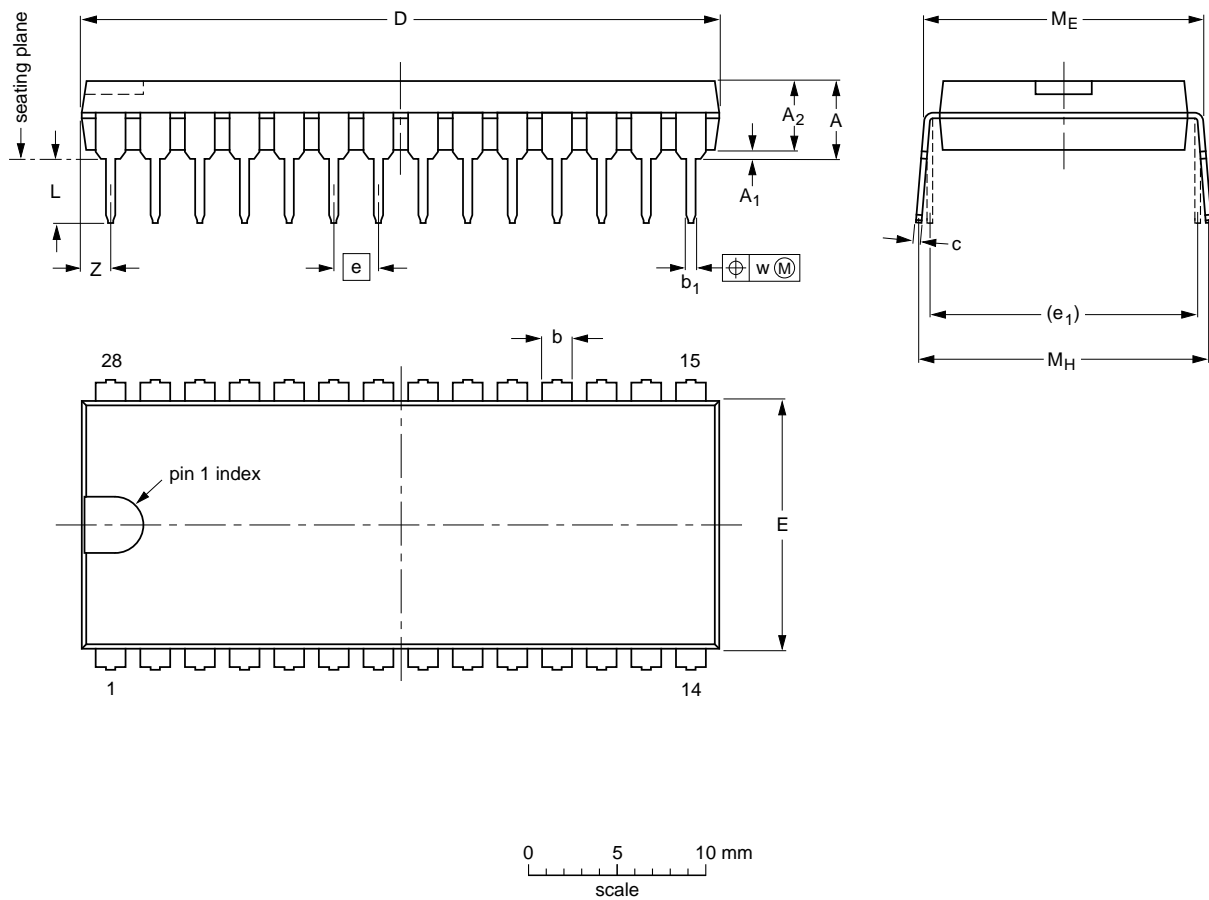
# Dual 16-bit DAC

# TDA1541

## PACKAGE OUTLINE

DIP28: plastic dual in-line package; 28 leads (600 mil)

SOT117-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				92-11-17 95-01-14

## Dual 16-bit DAC

## TDA1541

**SOLDERING****Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

**Soldering by dipping or by wave**

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**Repairing soldered joints**

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.